UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,968	09/25/2003	Peter G. Tolchinsky	42P16684	3614

8791 7590 10/30/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
SMITH, BRADLEY	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,968	TOLCHINSKY ET AL.	
	Examiner	Art Unit	
	Bradley K. Smith	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,9-11 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,9-11 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *search notes*.

DETAILED ACTION

Official Notice

1. Official notice is taken that silicon carbide (SiC) has a thermal conductivity that is greater than the thermal conductivity of silicon (Si). This is supported by the applicant's specification [0023] and Hummel (*Electronic Properties of Materials*) [Table 19.3].

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 6, 9, 10-12 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Kub et al. (2004/0224482). Kub et al. discloses forming a splitting layer in a semiconductor donor substrate (11); and depositing a bulk heat dissipation handle substrate(17) onto the semiconductor donor substrate, the bulk heat dissipation handle substrate having a thermal conductivity greater than that of said semiconductor donor substrate; and splitting said semiconductor donor substrate along said splitting layer after depositing said bulk heat dissipation handle substrate onto said semiconductor donor substrate (0044-0050). Regarding claim 2, Kub *et al.* further teaches a bulk heat dissipation substrate of SiC (0045).

Regarding claim 3, Kub *et al.* further teaches a bulk heat dissipation substrate which is a material that removes heat from the semiconductor substrate (inherent characteristic).

Regarding claims 5 and 6, Kub *et al.* further teaches forming the splitting layer by implanting hydrogen in the semiconductor substrate [0050].

Regarding claim 9, Kub *et al.* discloses using CVD to deposit the stiffening layer (0045).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 3, 5, 6, 9, 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub *et al.* in view of Ghyselen *et al.*

Kub *et al.* (US 6,323,108) teaches a process comprising forming a splitting layer **12** within the semiconductor substrate **10**, bonding the substrate directly to a bulk heat dissipation [column 4, lines 43-44] substrate **18** having a thermal conductivity greater than that of the substrate, and splitting the substrate along the splitting layer [column 6, line 41]. Kub *et al.* does not discuss depositing the bulk heat dissipation substrate by chemical vapor deposition (CVD). Ghyselen *et al.* (US 6,867,067) teaches depositing a SiC substrate [column 6, lines 60-65]. It would have been obvious to one of ordinary skill in the art to deposit the bulk heat dissipation substrate as taught by Ghyselen *et al.* in the method of Kub *et al.* since this alternate method of forming a bulk heat dissipation substrate provides improved growth rate and deposition parameter adjustment [column 7, lines 10-15].

Regarding claim 2, Kub *et al.* further teaches a bulk heat dissipation substrate of SiC [column 6, line 59].

Regarding claim 3, Kub *et al.* further teaches a bulk heat dissipation substrate which is a material that removes heat from the semiconductor substrate [column 6, lines 60-67].

Regarding claims 5 and 6, Kub *et al.* further teaches forming the splitting layer by implanting hydrogen in the semiconductor substrate [column 5, lines 55-65].

Regarding claims 9-12, Kub *et al.* does not discuss a chemical vapor deposition technique for depositing the SiC substrate. Ghyselen *et al.* teaches a CVD deposition method. It would have been obvious to one of ordinary skill in the art to use the CVD method of Ghyselen *et al.* in the method of Kub *et al.* since this method provides a low temperature method of depositing a SiC substrate as taught by Ghyselen *et al.*

Regarding claim 10, Kub *et al.* further teaches forming a transition layer on the bulk heat dissipation substrate which is silicon nitride or polysilicon [column 7, lines 5-10] and then bonding the transition layer to the substrate [Figure 1B].

4. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub *et al.* in view of Letertre *et al.*

Kub *et al.* teaches a process comprising providing a silicon wafer **10**, implanting hydrogen in the semiconductor substrate [column 5, lines 55-65; Figure 1A], bonding a SiC layer **18** [Figure 1B], and splitting the substrate along the implantation layer **12** [Figure 1C]. Kub *et al.* does not discuss depositing the SiC layer by CVD or polishing the silicon layer or SiC layer. Letertre *et al.* (US 6,815,309) teaches depositing a 0.5 mm thick SiC layer by using CVD [column 6, line 62; column 7, line 3] and polishing the SiC and Si layers [column 6, lines 5-10]. It would have been obvious to one of ordinary skill in the art use the SiC layer of Letertre *et al.* with the polishing steps in the method of Kub *et al.* since this provides a Si and SiC layers by a

typical deposition method with adjustable thicknesses which is compatible with further processing technologies.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kub *et al.* and Letertre *et al.* as applied to claim 15 above, and further in view of Lam *et al.*

Kub *et al.* as modified by Letertre *et al.* teach the limitations of claim 15 as described above, but they do not discuss the polished thickness of the SiC layer. Lam *et al.* (US 2005/0060115) teaches a 300 mm wafer which has a final thickness of 0.775 mm [0006]. It would have been obvious to one of ordinary skill in the art to polish the SiC layer to a thickness of between 0.75 mm and 0.8 mm since this is the industry standard thickness for 300 mm wafers.

Response to Arguments

Applicant's arguments filed 8/29/06 have been fully considered but they are not persuasive. The applicant contends that the invention is directed towards depositing a handle substrate, and that Kub, in contrast, is directed towards bonding a substrate. (Even though Kub teaches the CVD of SiC in paragraph 0045). The examiner would like to point out that the current specification discloses "The bulk heat dissipation substrate can also be deposited by a direct bonding method..." (see paragraph 0028 lines 8-10). Therefore the examiner understands the bonding method to be a method of depositing the handle substrate. The applicant further contends that a Kub disclose the stiffening layer is optional, and that Kub disclose different materials. But examiner would like to point out that Kub expressly discloses that SiC and that it can be used.

Applicant argues that Kub *et al.* does not teach a method of forming a splitting layer, depositing a bulk heat dissipation substrate, and then splitting the semiconductor substrate.

Applicant further argues that neither Ghyselen *et al.* , Letertre et al nor Lam *et al.* correct this deficiency. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Kub *et al.* teaches forming a splitting layer, bonding a bulk heat dissipation device, and splitting the substrate. Ghyselen *et al.* Letertre et al. and Lam *et al.* are used to provide the missing step of depositing the bulk heat dissipation device as an alternate method to the bonding method of Kub *et al.* The further teachings of Letetre *et al.* and Lam *et al.* regarding substrate processing are irrelevant to this combination since they do not teach away from the combination of Kub *et al.* with Letertre *et al.* or Kub *et al.* with Lam *et al.* These combinations teach all the limitations of the claimed invention as describe above. The analysis of each reference individually does not overcome the rejections based on a combination of the references.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is 571-272-1884. The examiner can normally be reached on 10-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Bradley K Smith
Primary Examiner
Art Unit 2891